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TECHNISCHE FAKULTÄT

Elektrotechnik-Elektronik-Informationstechnik

EEI KOLLOQUIUM

Circuit Topologies and Design Methodologies for High Data-Rate mm-Wave Radio Transceivers in SOI and FDSOI CMOS

Prof. Sorin Voinigescu
University of Toronto, Kanada

Montag, der 09.10.2017, 16^{00} Uhr
Cauerstraße 9, Tietze-SchenkSaal

Diskussionsleitung: Prof. Dr.-Ing. R. Weigel

This presentation will explore fully digital architectures and circuit topologies for future wireless backhaul systems with aggregate data rates comparable to those of future 64Gbaud fiberoptic systems. The main features of FD-SOI CMOS technology and how to efficiently use its unique features for RF and mm-wave SoCs will be reviewed first. We will discuss the impact of the back-gate bias on the measured I-V, transconductance, fT and fMAX characteristics and compare the MAG of FDSOI MOSFETs with those of planar bulk CMOS, SOI and SiGe BiCMOS transistors through measurements up to 325 GHz. I will provide examples of FDSOI LNA, mixer, switches, and PA circuit topologies and layouts that make efficient use of the back-gate bias to overcome the limitations associated with the low breakdown voltage of sub-28nm CMOS technologies. Examples of measured 45nm SOI CMOS digital transmitters with free space constellation formation at 100 GHz and 140 GHz will be provided along with a 1-30GHz fully digital I-Q transmitter with 20 dBm output power for 5G terminals. Finally, Predistortion and spectral shaping techniques in the transmitter, and receiver ADC-based equalization at 64 GBaud will be discussed.