KOLLOQUIUM

Institut für Elektrotechnik, Elektronik und Informationstechnik

Design of High-End SAR ADCs

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Until the year 2000, Analog-to-Digital Converters (ADC) based on the principle of successive approximation (SAR) were mostly designed with the basic principle. The analog input voltage Vin is compared to partitions of a reference voltage REF, which are generated with a Digital-to-Analog Converter (DAC). In this way, the input voltage is first compared to half of reference voltage. If the input voltage is higher, then it is compared to three quarters of the reference voltage in the next step, otherwise to one quarter. The DAC voltage is converging successively to the analog input voltage. The digital input to the DAC in the end of the conversion is identical to the digitized input voltage of the ADC, so that the accuracy of the SAR converter relies totally on the performance of the DAC. The design of the sample and hold stage (S&H) was done fully differential to reject noise and charge injection. Different trim solutions were implemented to get highest performance DACs and the comparator worked with offset cancellation.

ADCs are typically designed on a 5V or 3V process to keep the input voltage range high. The smaller the input span, the more sensitive is the signal path for noise injection, supply or ground ripples. This sets a limitation to the performance of the converter in respect to speed and power consumption. The high-end products achieved 16bit resolution with up to 500kSPS and consumed typically 100mW. The differential non-linearity (DNL) was limited to 14-15bit, the integral non-linearity (INL) to 13-14bit and the signal-to-noise ratio (SNR) to 83-85dB.

Since then, the research was pushing towards new and exciting architectures, so that state-of-the-art products run all the way up to 4MSPS at a 16bit resolution and a power dissipation of 155mW, or 1MSPS with 18bit resolution and 225mW. The differential linearity is truly 16bit; the integral linearity up to 16bit with an SNR that reaches up to 96dB.

The research work of the last years is presented on the example of two SAR ADCs. The first 16bit ADC concentrates on the reduction of the power dissipation (15.5mW at 1MSPS) and optimizes the performance for linearity and noise. The second ADC is the high speed 4MSPS 16bit converter from above.